



15. (Amended) A data processing device according to Claim 14, wherein said [second] first description held in said [third] first register can be variably set.

16. (Amended) A data processing device according to Claim 14, further comprising:

a program counter which sequentially counts an address corresponding to each of the plurality of instructions and holds the address, wherein an address value is held in said [third] first register as said [second] first description; and

$a^3$  said instruction execution unit, detects an event that the address value held in said [third] first register is in agreement with an address of said program counter and starts to [judge] determine whether or not said condition is satisfied in response to the detection.

17. (Amended) A data processing device according to Claim [15] 25, wherein said conditional instruction has a field for designating an operation which designate contents of the operation, a field for designating condition which designates the executing condition of the operation and a field for designating an amount of delay which designate a [time] timing for [judging] determining the execution condition;

said instruction decoder produces said first control signal based on contents described in said field for designating operation, outputs the second description in accordance with the contents described in said field for designating the condition [as said first description] and outputs the contents described in said field for designating the amount of delay;